STK7000

N-Channel Enhancement-Mode MOSFET

Description

- High speed switching application.

Features

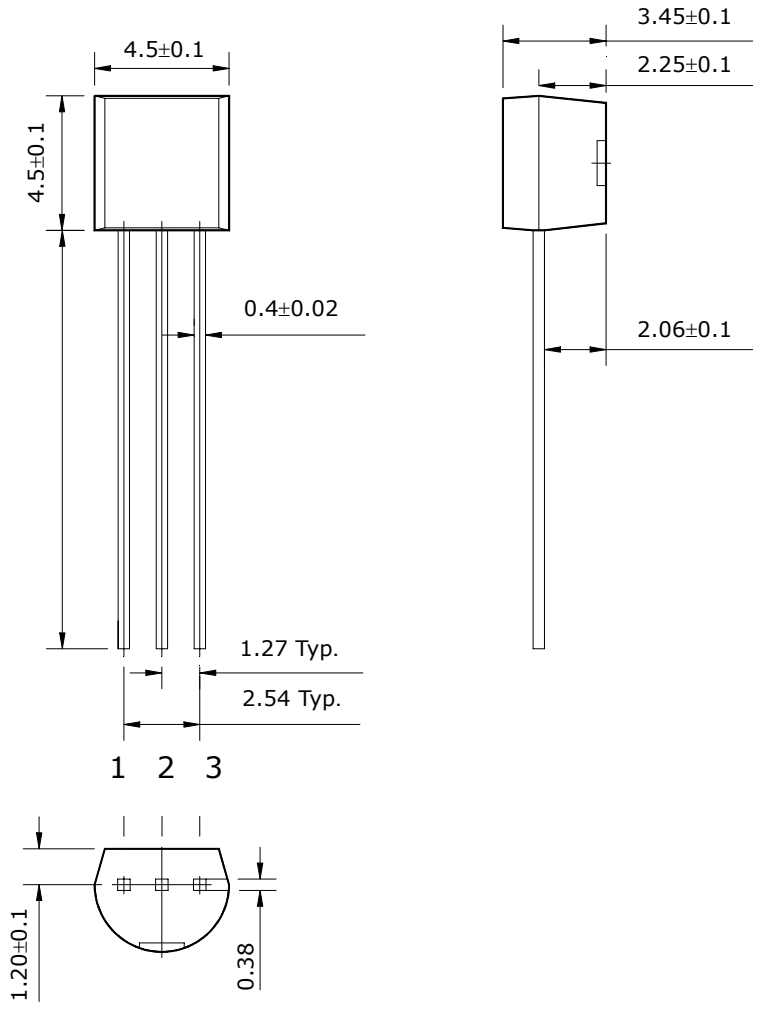
- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch
- High saturation current capability.

Ordering Information

Type NO.	Marking	Package Code
STK7000	STK7000	TO-92

Outline Dimensions

unit : mm



PIN Connections
1. Source
2. Gate
3. Drain

Absolute maximum ratings (Ta=25°C)

Characteristic	Symbol	Ratings	Unit
Drain-Source voltage	V_{DSS}	60	V
Gate-Source voltage	V_{GS}	±20	V
Maximum Drain current	I_D	200	mA
Pulsed Drain Current	I_{DP} *	500	mA
Power dissipation	P_D	400	mW
Maximum Junction-to-Ambient	R_{thJA}	312.5	°C/W
Operating Junction and Storage temperature range	T_J , T_{stg}	-55~150	°C

* PW ≤ 10 μs, Duty cycle ≤ 1%

Electrical Characteristics (Ta=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drian-Source breakdown voltage	BV_{DSS}	I_D=10μA, V_{GS}=0	60	-	-	V
Gate-Threshold voltage	$V_{GS(th)}$	I_D=0.25mA, V_{DS}=V_{GS}	0.8	2.1	3	V
Zero Gate voltage drain current	I_{DSS}	V_{DS}=50V, V_{GS}=0	-	-	1	μA
Gate-body leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
Drain-Source on-resistance	$R_{DS(ON)}$ *	V_{GS}=5V, I_D=50mA	-	4.5	5.3	Ω
		V_{GS}=10V, I_D=500mA	-	2.4	5.0	Ω
		T_J=125℃	-	4.4	9	Ω
Forward transconductance	g_{fs}	V_{DS}=10V, I_D=0.2A	100	-	-	mS
Input capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0, f=1MHz	-	22	60	pF
Output capacitance	C_{oss}	V_{DS}=25V, V_{GS}=0, f=1MHz	-	11	25	pF
Reverse Transfer capacitance	C_{rss}	V_{DS}=25V, V_{GS}=0, f=1MHz	-	2	5	pF
Turn-on time	t_{ON}	V_{DD}=15V, I_D=0.5A V_{GS}=10V, R_G=25Ω	-	-	10	ns
Turn-off time	t_{OFF}	V_{DD}=15V, I_D=0.2A V_{GS}=10V, R_G=25Ω	-	-	10	ns

* PW ≤ 300 μs, Duty cycle ≤ 1%

Electrical Characteristic Curves

Fig. 1 I_D - V_{DS}

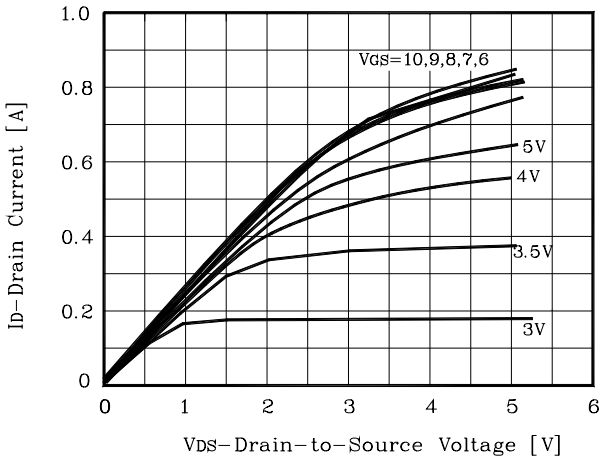


Fig. 2 I_D - V_{GS}

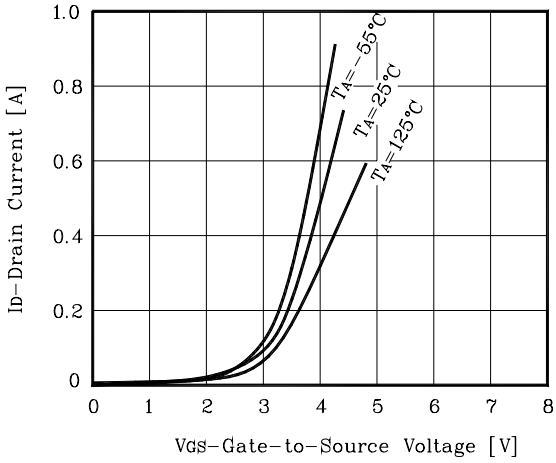


Fig. 3 $R_{DS(on)}$ - I_D

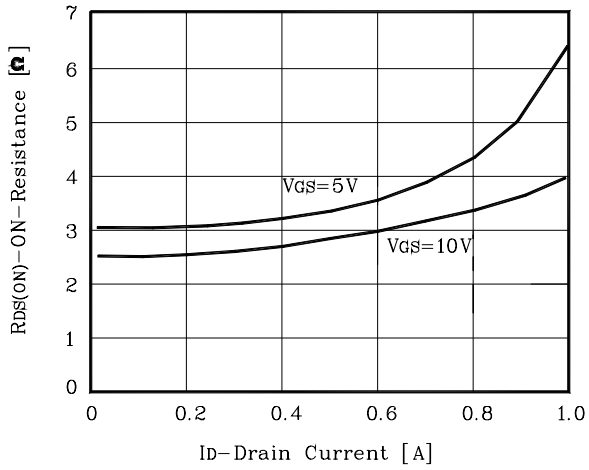


Fig. 4 C - V_{DS}

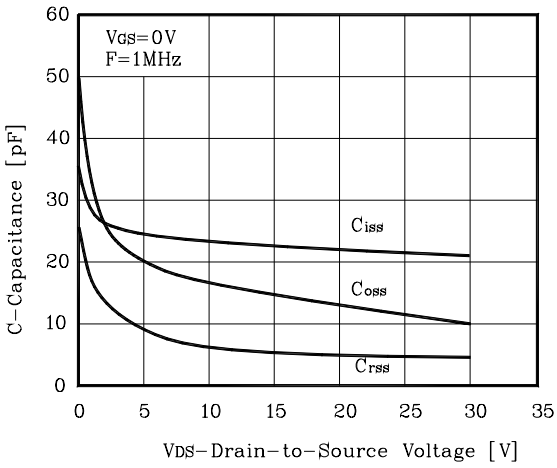


Fig. 5 V_{GS} - Q_g

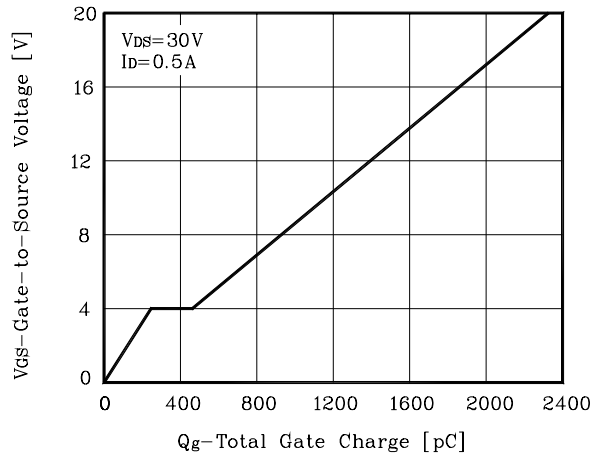


Fig. 6 $R_{DS(on)}$ - T_J

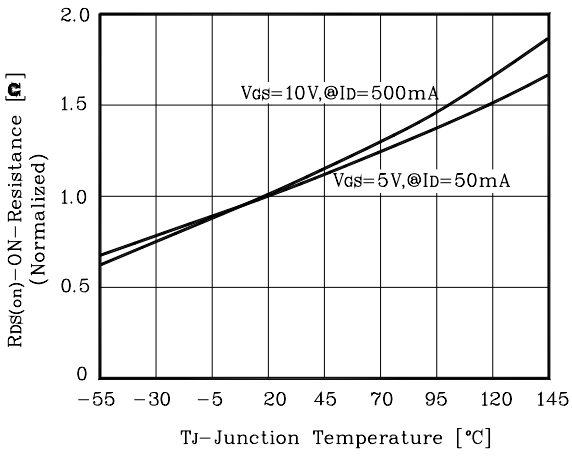


Fig. 7 $R_{DS(on)}$ - V_{GS}

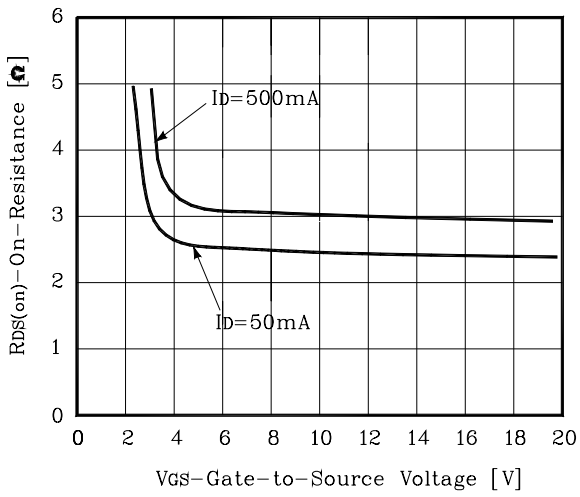


Fig. 8 I_S - V_{SD}

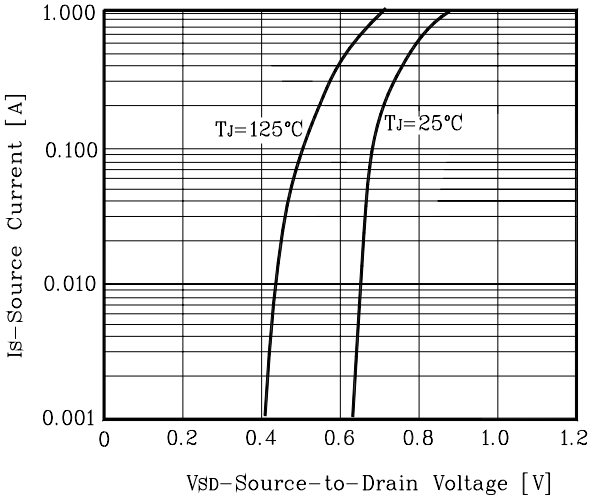
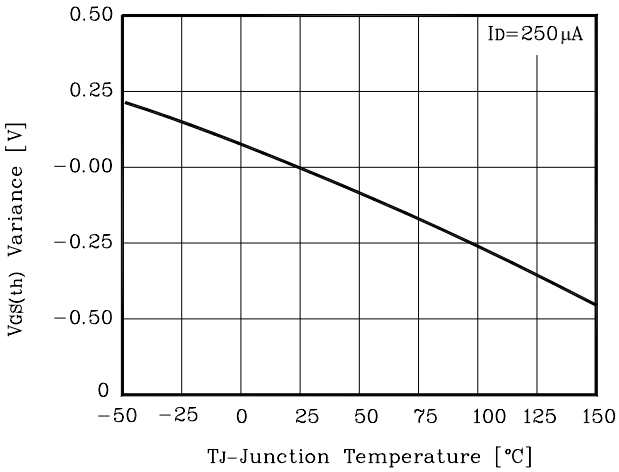


Fig. 9 $V_{GS(th)}$ - T_J



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