

Portable Equipment Application.

Notebook Application.

Features

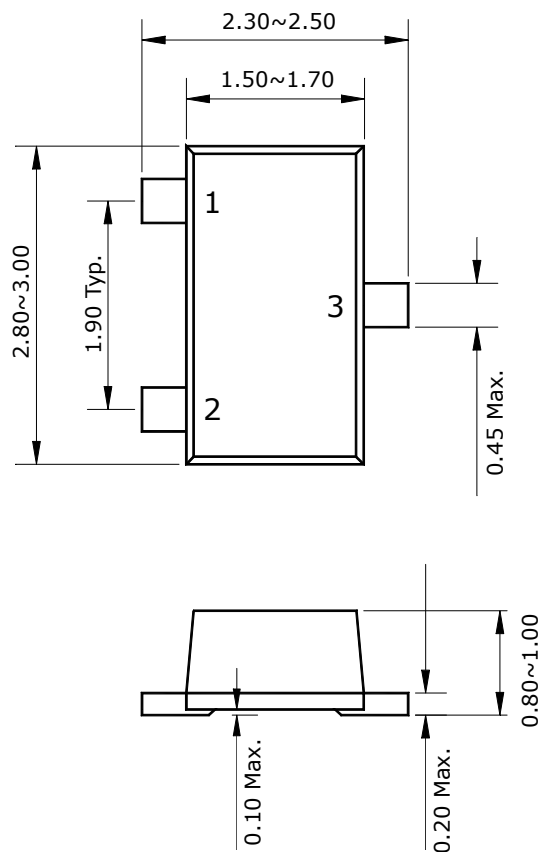
- Low $V_{GS(th)}$: $V_{GS(th)} = -0.6 \sim -1.4V$
- Small footprint due to small package
- Low $R_{DS(ON)}$: $R_{DS(ON)} = 68m\Omega$ (Typ.)

Ordering Information

| Type NO. | Marking | Package Code |
|----------|---------|--------------|
| STJ001SF | J01 | SOT-23F |

Outline Dimensions

unit : mm



PIN Connections

1. Gate
2. Source
3. Drain

Absolute maximum ratings

(Ta=25°C)

| Characteristic | Symbol | Rating | Unit |
|----------------------------------|-----------|---------|------|
| Drain-source voltage | V_{DSS} | -20 | V |
| Gate-source voltage | V_{GSS} | ±12 | V |
| Drain current (DC) ** | I_D | -2.8 | A |
| Drain current (Pulsed) * | I_{DP} | -11.2 | A |
| Total Power dissipation ** | P_D | 0.5 | W |
| Avalanche current (Single) ② | I_{AS} | -2.8 | A |
| Single pulsed avalanche energy ② | E_{AS} | 28 | mJ |
| Avalanche current (Repetitive) ① | I_{AR} | -2.8 | A |
| Repetitive avalanche energy ① | E_{AR} | 1.3 | mJ |
| Junction temperature | T_J | 150 | °C |
| Storage temperature range | T_{stg} | -55~150 | |

* Limited by maximum junction temperature

** Device mounted on a glass-epoxy board

| Characteristic | | Symbol | Typ. | Max | Unit |
|--------------------|------------------|------------------|------|-----|------|
| Thermal resistance | Junction-ambient | $R_{th(J-a)}$ ** | - | 250 | °C/W |

P-CH Electrical Characteristics

(Ta=25°C)

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit | |
|--------------------------------|--------------|--|------|------|-----------|------------|-----|
| Drain-source breakdown voltage | BV_{DSS} | $I_D = -250\mu A, V_{GS} = 0$ | -20 | - | - | V | |
| Gate threshold voltage | $V_{GS(th)}$ | $I_D = -250\mu A, V_{DS} = V_{GS}$ | -0.6 | - | -1.4 | V | |
| Drain-source cut-off current | I_{DSS} | $V_{DS} = -20V, V_{GS} = 0V$ | - | - | 1 | μA | |
| Gate leakage current | I_{GSS} | $V_{DS} = 0V, V_{GS} = \pm 12V$ | - | - | ± 100 | nA | |
| Drain-source on-resistance | $R_{DS(on)}$ | $V_{GS} = -5.0V, I_D = -1.4A$ | - | 68 | 88 | m Ω | |
| | | $V_{GS} = -2.5V, I_D = -1.4A$ | - | 72 | 93 | m Ω | |
| Forward transfer conductance ④ | g_{fs} | $V_{DS} = -5V, I_D = -2.8A$ | - | 15 | - | S | |
| Input capacitance | C_{iss} | $V_{GS} = 0V, V_{DD} = -10V,$ $f = 1MHz$ | - | 880 | 1320 | pF | |
| Output capacitance | C_{oss} | | - | 210 | 320 | | |
| Reverse transfer capacitance | C_{rss} | | - | 110 | 170 | | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = -10V, I_D = -2.8A$ $R_G = 10\Omega$ | - | 5.2 | - | ns | |
| Rise time | t_r | | - | 10 | - | | |
| Turn-off delay time | $t_{d(off)}$ | | ③④ | - | 17.6 | | - |
| Fall time | t_f | | - | 10 | - | | |
| Total gate charge | Q_g | $V_{DD} = -10V, V_{GS} = -5V$ $I_D = -2.8A$ | - | 8.0 | 12 | nC | |
| Gate-source charge | Q_{gs} | | ③④ | - | 1.3 | | 2.0 |
| Gate-drain charge | Q_{gd} | | - | - | 2.3 | | 3.5 |

Source-Drain Diode Ratings and Characteristics

(Ta=25°C)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------|----------|---|-----|------|------|---------|
| Source current | I_S | Integral reverse diode in the MOSFET | - | - | -0.5 | A |
| Sourcecurrent(Plused) ① | I_{SM} | | - | - | -2.8 | |
| Forward voltage ④ | V_{SD} | $V_{GS} = 0V, I_S = -0.5A$ | - | -0.9 | -1.3 | V |
| Reverse recovery time | t_{rr} | $I_S = -0.5A$ | - | 73 | - | ns |
| Reverse recovery charge | Q_{rr} | $di_s/dt = 100A/us$ | - | 250 | - | μC |

Note ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② $L = 2.0mH, I_{AS} = -2.8A, V_{DD} = -10V, R_G = 25\Omega$
- ③ Pulse Test : Pulse Width < 300us, Duty cycle $\leq 2\%$
- ④ Essentially independent of operating temperature

P-CH Electrical Characteristic Curves

Fig. 1 $I_D - V_{DS}$

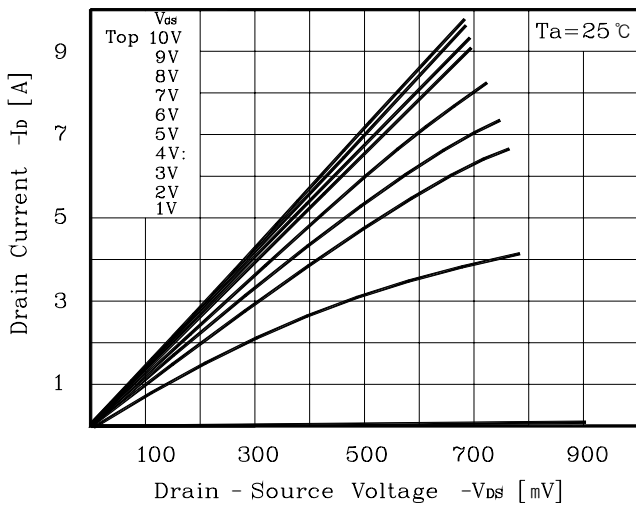


Fig. 2 $I_D - V_{GS}$

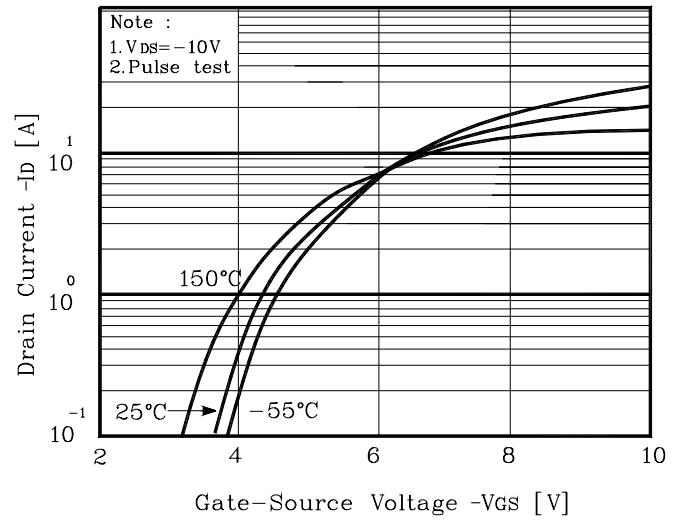


Fig. 3 $R_{DS(on)} - I_D$

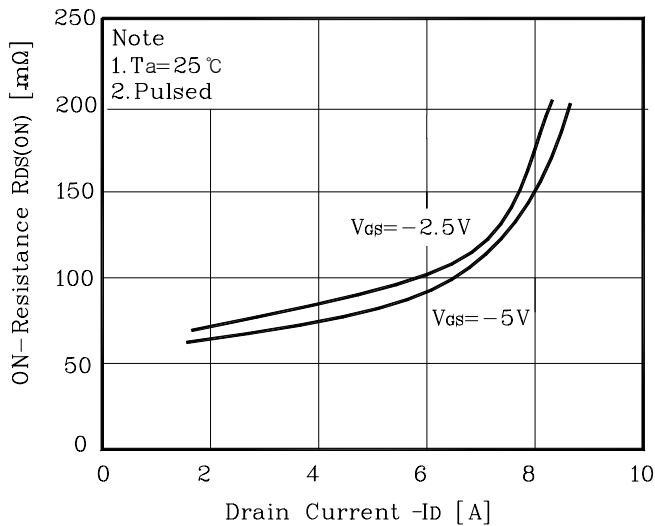


Fig. 4 $I_S - V_{SD}$

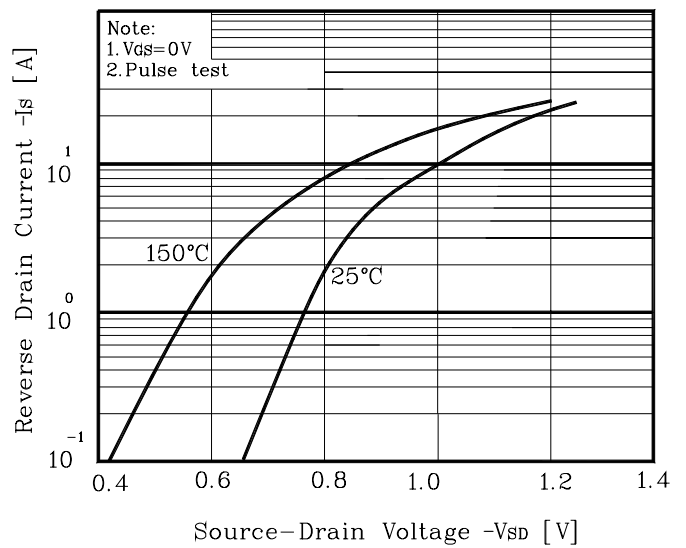


Fig. 5 Capacitance - V_{DS}

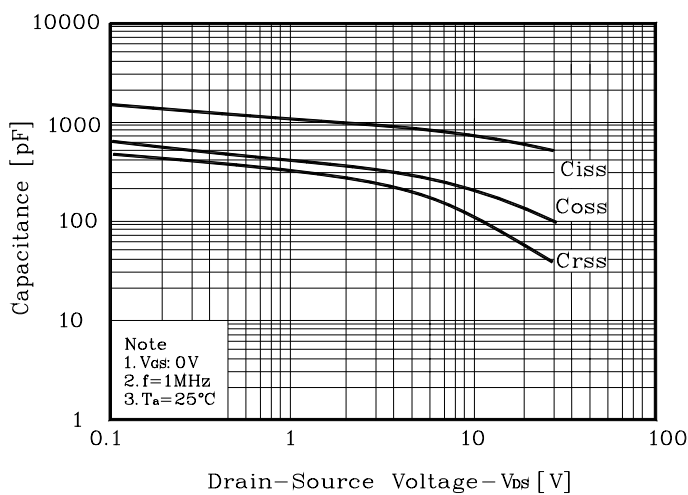


Fig. 6 $V_{GS} - Q_G$

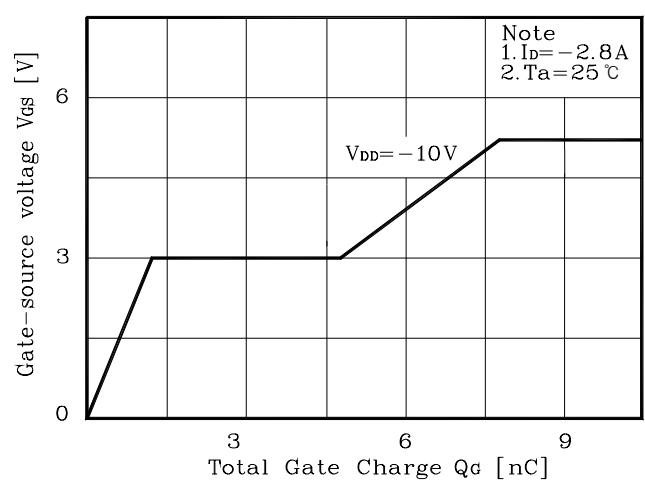


Fig. 7 $V_{DSS} - T_J$

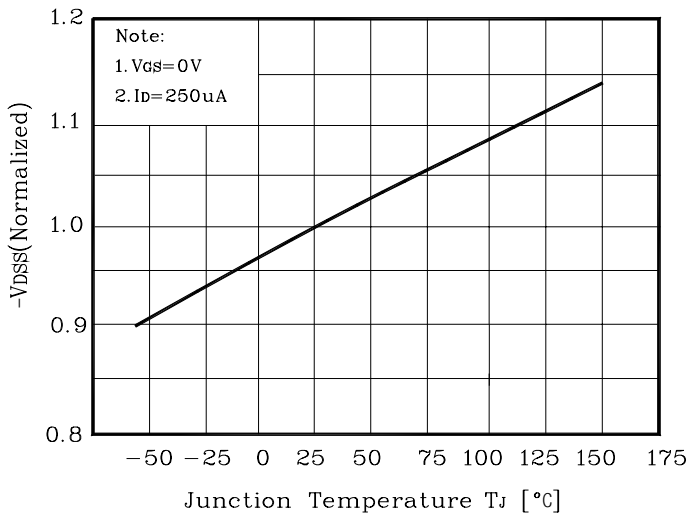


Fig. 8 $R_{DS(on)} - T_J$

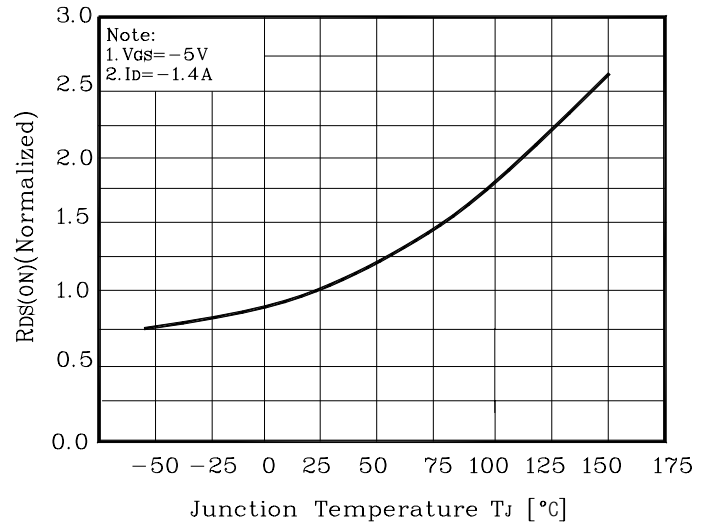


Fig. 9 $I_D - T_a$

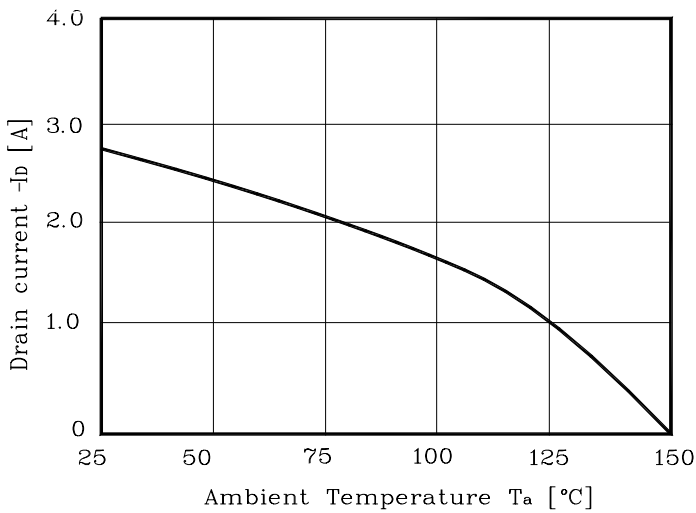


Fig. 10 Safe Operating Area

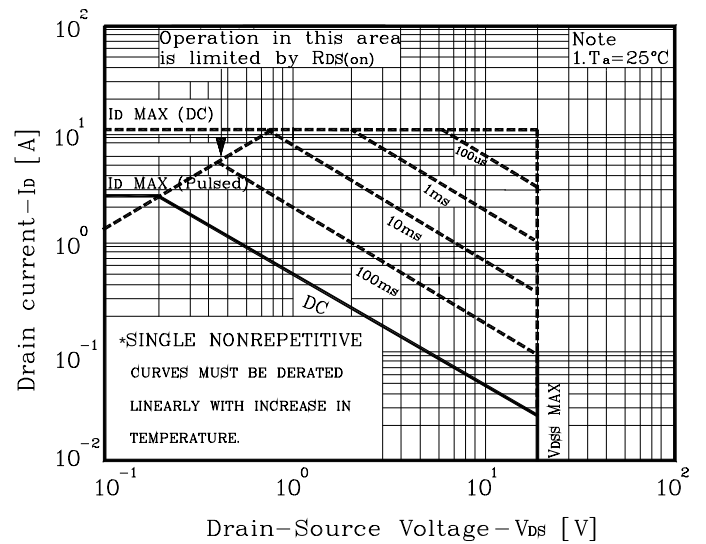


Fig. 11 Gate Charge Test Circuit & Waveform

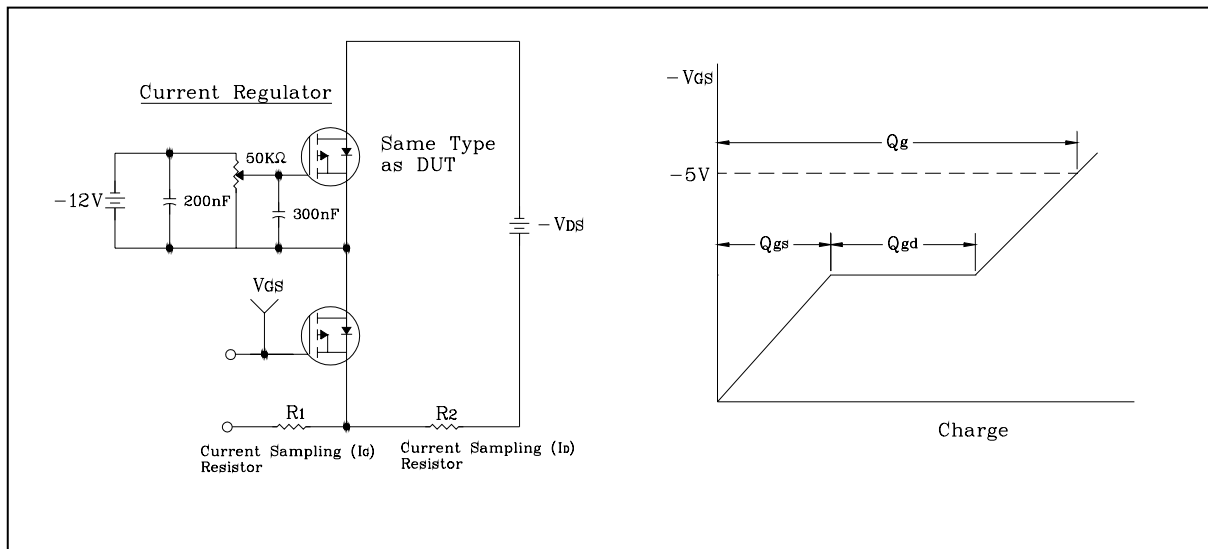


Fig. 12 Resistive Switching Test Circuit & Waveform

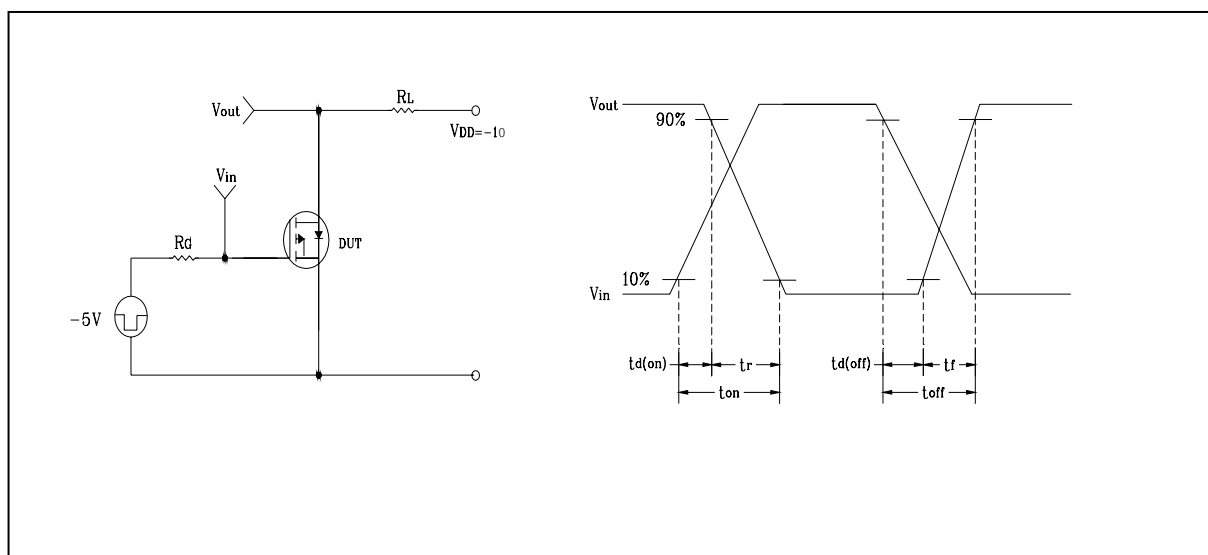


Fig. 13 EAS Test Circuit & Waveform

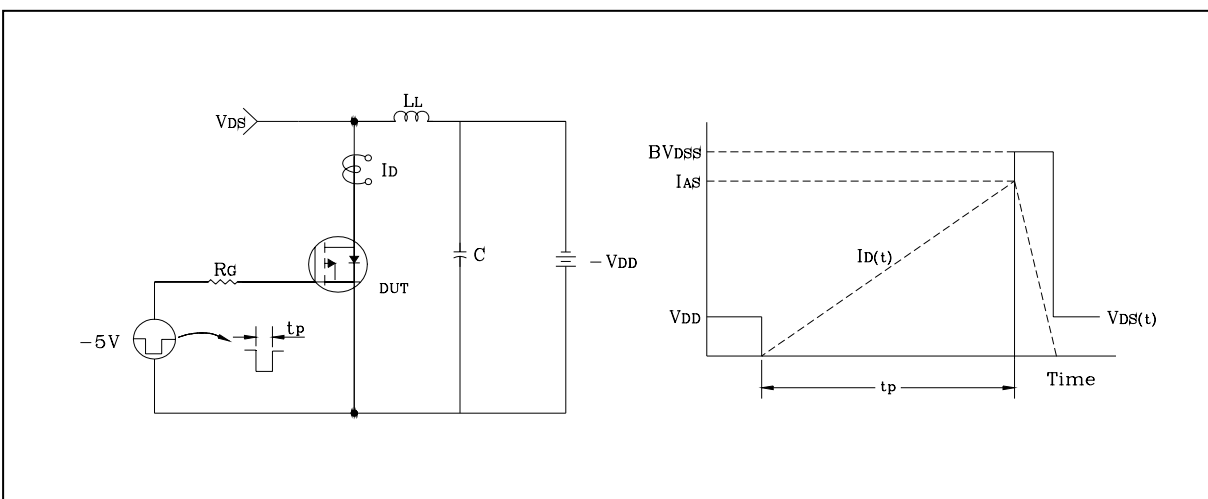
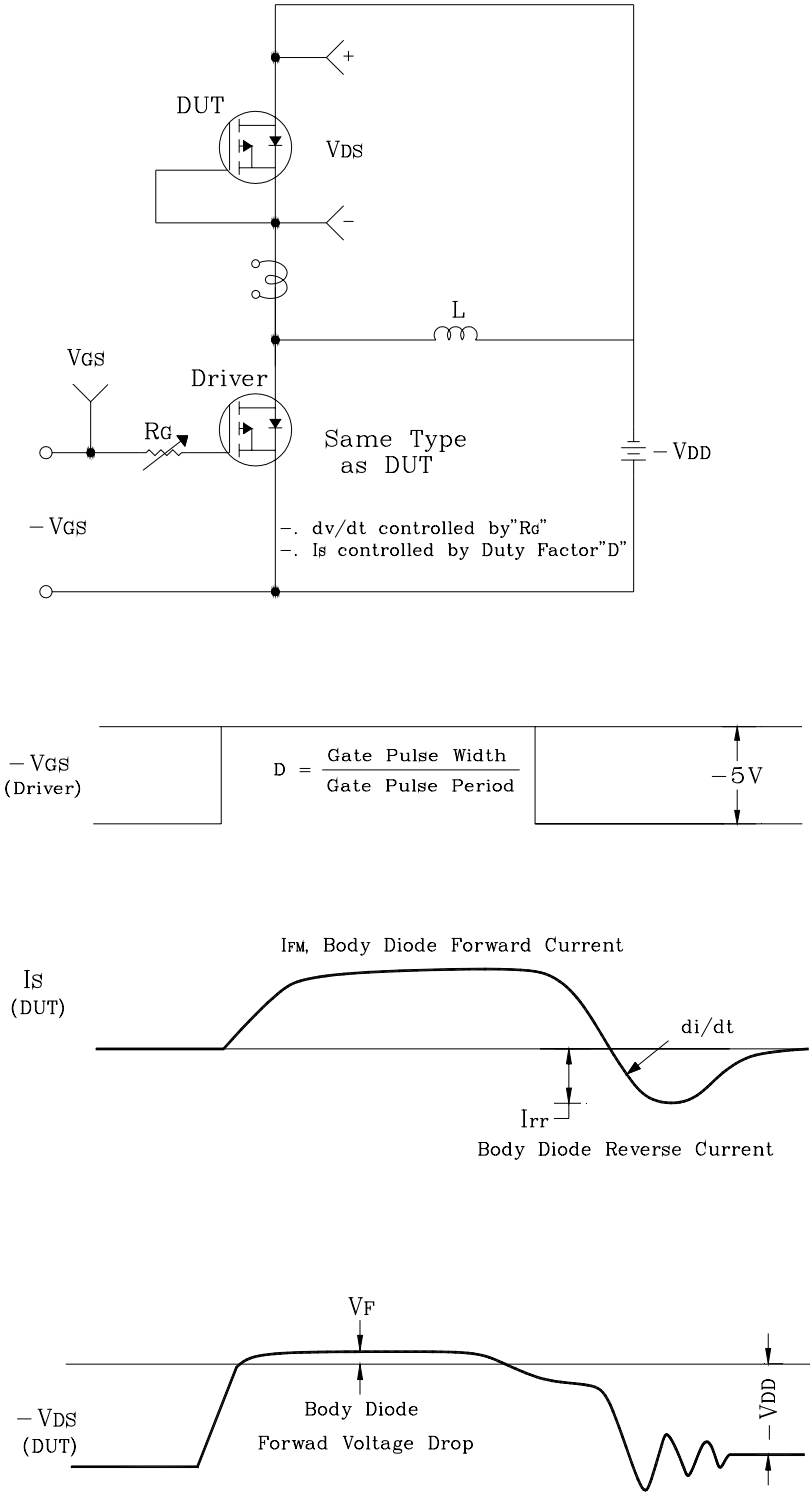


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



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