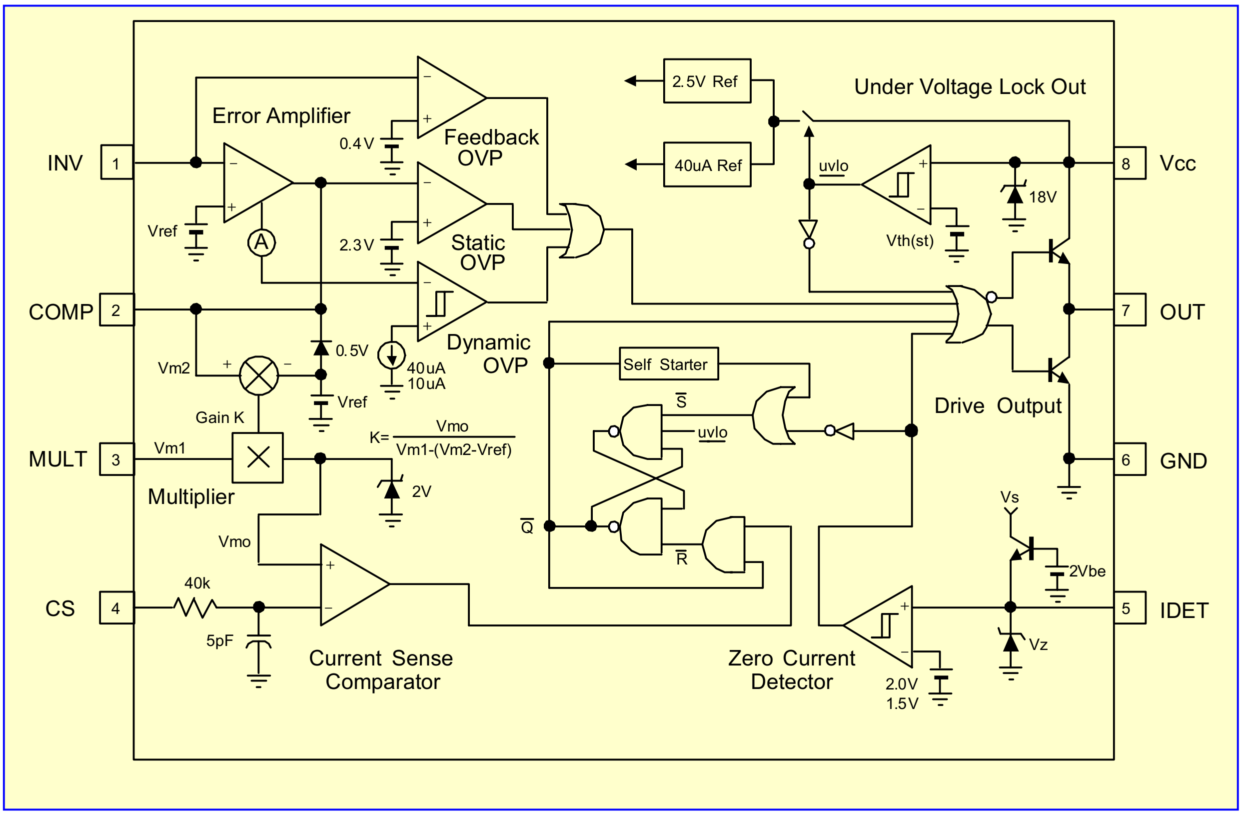
1. Introduction

The TM (Transition Mode) technique is widely used for Power Factor Correction in low power applications, such as lamp ballasts or low-end monitors. The S6500 is the latest AUK's proposal for this market and the emerging ones that are supposed to require a low-cost Power Factor Correction.
Based on a well-established architecture, the S6500 offers excellent performance that enlarges its field of application considerably.

The front-end stage of conventional off-line converters, typically made up of a full wave rectifier bridge with a capacitor filter, gets an unregulated DC bus from the AC mains. The filter capacitor must be large enough to have a relatively low ripple superimposed on the DC level.
This means that the instantaneous line voltage is below the voltage on the capacitor most of the time, thus the rectifiers conduct only for a small portion of each line half-cycle. The current drawn from the mains is then a series of narrow pulses whose amplitude is 5-10 times higher than the resulting DC value.
Lots of drawbacks result from that: much higher peak and RMS current drawn from the line, distortion of the AC line voltage, over currents in the neutral line of the three-phase systems and, after all, a poor utilization of the power system's energy capability.
This can be measured in terms of either harmonic contents, as norms EN61000-3-2 envisage, or Power Factor (PF), intended as the ratio between the real power (the one transferred to the output) and the apparent power (RMS line voltage times RMS line current) drawn from the mains, which is more immediate.
A traditional input stage with capacitive filter has a low PF (0.5-0.7) and high harmonic contents.
By using switching techniques, a Power Factor Corrector (PFC) pre-regulator, located between the rectifier bridge and the filter capacitor, allows drawing from the mains a quasi-sinusoidal current, in-phase with the line voltage.
The PF becomes very close to 1 (more than 0.99 is possible) and the aforesaid drawbacks are eliminated.
Theoretically, any switching topology can be used to achieve a high PF but, in practice, the boost topology has become the most popular because of the advantages it offers:
1) mainly, the circuit requires the fewest external parts, thus it is the cheapest. Additionally:
2) the boost inductor located between the bridge and the switch causes the input di/dt to be low, thus minimizing the noise generated at the input and, therefore, the requirements on the input EMI filter;
3) the switch is source-grounded, therefore is easy to drive.

However, boost topology requires the DC output voltage to be higher than the maximum expected line peak voltage (400V DC is a typical value for 220V or wide range mains applications). Besides, there is no isolation between input and output, thus any line voltage surge will be passed on to the output.
Two methods of controlling a PFC pre-regulator are currently widely used : the fixed frequency average current mode PWM and the Transition Mode (TM) PWM (fixed ON-time, variable frequency).
one requires a simpler control (implemented by AUK's S6500), much fewer external parts and is therefore much less expensive. With the first method the boost inductor works in continuous conduction mode, while TM makes the inductor work on the boundary between continuous and discontinuous mode, by definition.
For a given throughput power, TM operation then involves higher peak currents. This, also consistently with cost considerations, suggests its use in a lower power range (typically below 150W), while the former is recommended for higher power levels.

Figure 1. Block Diagram of the S6500.



S6500 PFC Controller Integrated Circuit

The S6500, whose internal block diagram is shown in fig. 1, is an IC intended to control PFC preregulators by using the Transition Mode technique. The device is available in DIP-8 and SOP-8 Packages.

The most significant features of the S6500 concern the following points:

- Dynamic, Static & Feedback OVP
- Extremely low start up current (30μA typ. , 50μA guaranteed) for simple start-up circuits (just one resistor) with very low power dissipation;
- Very low operating current (4mA Typ.)
- Internal self start timer
- On-chip RC filter on the current sense pin ➔ CS
- Trimmed ±1.5% internal Reference
- Under voltage lock out with hysteresis
- Multiplier with extended dynamics for wide range mains applications, with excellent THD
- Pin Compatible to World Standard
- Totem pole output stage is capable of driving a power MOS or IGBT with source and sink current of $\pm$500mA.

The IC is optimised for controlling PFC preregulators based on boost topology in electronic lamp ballasts, AC-DC adapters and low power (<150 W) SMPS.

However, its excellent performance along with the extremely reduced external parts count allows also the use in unconventional topologies/applications.

2. Device Blocks Description

SUPPLY BLOCK

As shown in fig. 1, a linear voltage regulator supplied by Vcc generates an internal 7V rail used to supply the whole integrated circuit, except for the output stage which is supplied directly from Vcc. In addition, a bandgap circuit generates the precise internal reference (2.5V±1.5% @ 25°C) used by the control loop to ensure a good regulation.

Figure 2. Internal Supply Block.

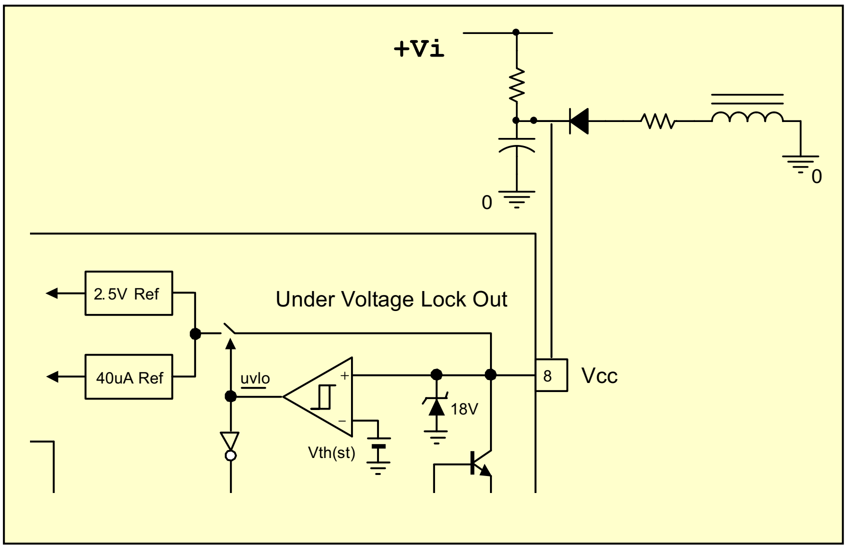


fig.2 is shown the undervoltage lockout (UVLO) comparator with hysteresis used to enable the chip as long as the Vcc voltage is high enough to ensure a reliable operation.

ERROR AMPLIFIER AND OVERVOLTAGE DETECTOR BLOCK (see fig. 3 and 4):

The Error Amplifier (E/A) inverting input, through an external divider connected to the output bus, compares a partition of the boosted output DC voltage, Vo, with the internal reference, so as to maintain the pre-regulator output DC voltage constant. The E/A output is used for frequency compensation, usually realised with a feedback capacitor connected to the inverting input.

The E/A bandwidth will be extremely low because the output of the E/A must be constant over a line half - cycle to achieve high PF.

The dynamics of the E/A output is internally clamped so that it can swing between 2V and 5.8V in order to speed up the recovery after the E/A saturates low due to an overvoltage or saturates high because of an overcurrent.

The device is provided with a two-level overvoltage protection (OVP), realized by using the pin connected to the E/A output.

In case of overvoltage, the output of the E/A will tend to saturate low but the E/A response is very slow, so it will take a long time to go into saturation. On the other hand, an overvoltage must be corrected immediately.

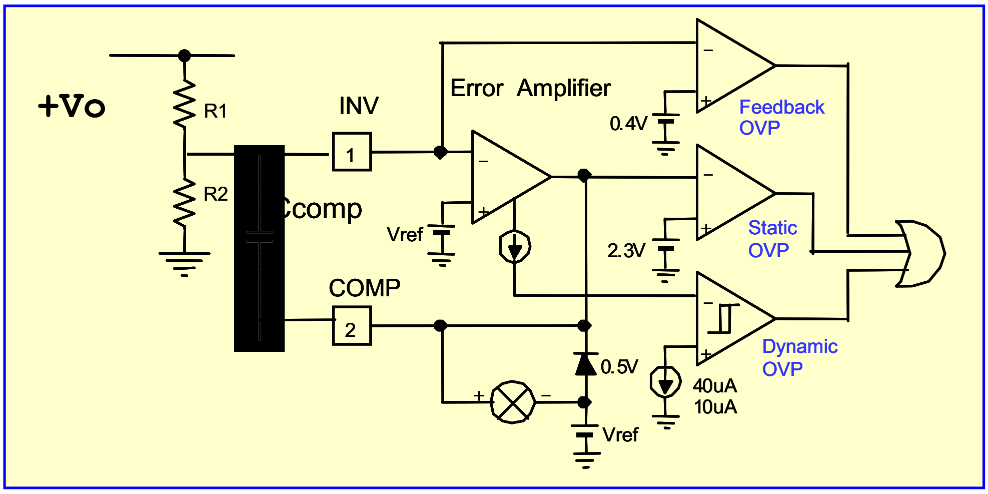
Hence a fast OVP detector, based on a different concept, is necessary.

In steady state condition, the current through R1 is equal to the current in R2 because the compensation capacitor does not allow DC current to flow (neither does the high-impedance inverting input of the E/A)

$$I_{R1,R2} = \frac{V_O - 2.5}{R1} = \frac{2.5}{R2}$$

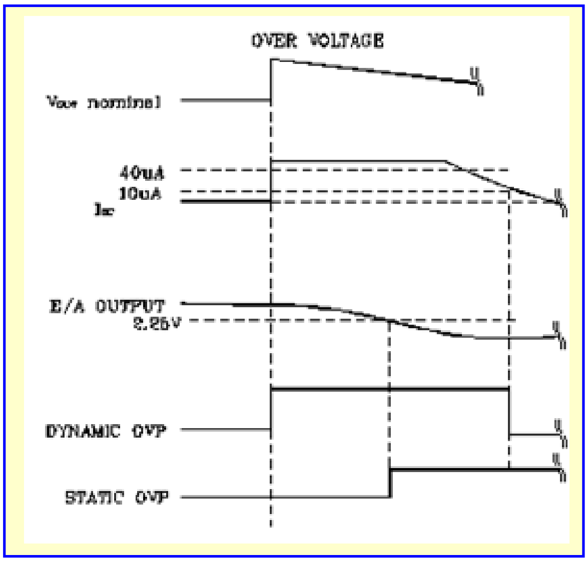
When the output voltage rises because of a step load change, the current in R1 builds up as well but the current through R2, fixed by the internal 2.5V reference, does not because of the E/A slowness. The current in excess will then flow through the feedback capacitor and enter the low-impedance E/A output, where it is sensed. In case, a two-step procedure can occur.

Figure 3. Error Amplifier and Overvoltage Detector Block.



When the current in excess reaches about 37μA, the output voltage of the multiplier is forced to decrease thus the energy drawn from the mains is reduced. This slows down the rate of rise of the output voltage. In some cases, this "soft braking" action is able to prevent the output voltage from exceeding the regulated value too much. If the output voltage further increases despite the soft braking, so that the current entering the E/A reaches 40μA, a "sharp braking" takes place. The output of the multiplier is pulled to ground, thus turning off the output stage and the external MOSFET. Also the internal starter is switched off. The internal current comparator is provided with hysteresis, thus the pull-down will be released and the output stage re-enabled as the current entering the E/A falls approximately below 10μA.

Figure 4. Dynamic and Static OVP operation.

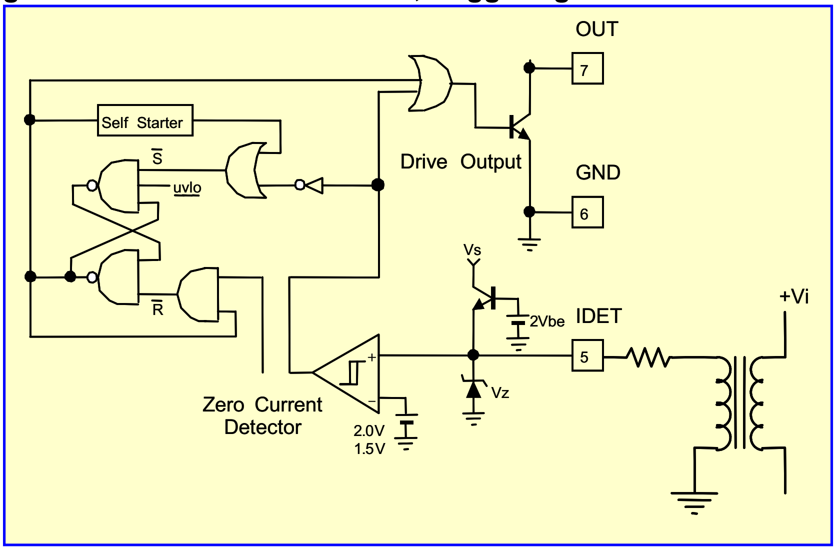


Static & Feedback OVP
OVP is cosisted of 3 parts that Dynamic OVP which controls an instant over-voltage of Boost Converter, Static OVP which operates prtection by sensing the out-put voltage under 2.3V from Error Amplifier after Dynamic OVP and OVP which is Grand short of INV in Feedback Input or Loop Fault in Feedback.
Static OVP is a different protection to Feedback OVP. Static OVP related with Dynamic OVP is operating almost continuously with Dynamic OVP After the state when out-put of Error Amplifier is low and unable to flow 40μA to Compensation Capacitor thus OVP doen't drive due to infelicitous Output Condition.
The Static OVP is needed for the case above. The Static OVP is needed to operate OVP continuously after Dynamic OVP from OVP Condition.
Feedback OVP has the operation function consisted of Resistances of Feedback Loop which are consisted of out-put and Resistance(R1) connected to INV, and INV and Resistance(R2) connected to GND.
When R1 is open Feedback INV is connected to GND through R2, OVP consequently recognise Feedback signal as the out-put of Boost Converter is low. So Error Amplifier controls switching with it's high out-put as it's maxium responsibility.
In consequence of operation above there is no method to control over out-voltage of Boost Converter the Switch is burnt out. The Feedback OVP can only under-control the condition of situation above.
Feedback OVP makes the Out-put low when it recongnise in-put of INV is under 0.4V. With the pratical application above it can control the protection for exterior parts by connecting INV. One of most importances is that it can delay the OVP signal by Delay timer for 1.5 ~ 1.8 μS. It contributes strength of specific noise charater toward Error Amplifier. Therefore the practical application can prevent the phenomenon that whole control loop gets unsteable from OVP mis-operation occured by noise causing from exterior condition.

Fig. 4 illustrates the combined action of dynamic and static OVP.
This dynamic OVP, with its combination of soft and sharp braking, is effective to handle most of load changes but does not provide a complete protection. In fact it is sensitive to output voltage variations (whence the appellative "dynamic") and cannot reveal a steady overvoltage, which is likely to occur in case of load disconnection.
The above mentioned concept of the E/A saturation is effective to achieve a "static" OVP. If the overvoltage lasts so long that the output of E/A goes below 2.25V (the E/A is in linear dynamics up to 2.5V), the protection is activated. Besides turning off the output stage and the external MOSFET, it disables some internal blocks reducing the quiescent current of the chip to 1.4mA (typ). The operation of the device is re-enabled as the E/A output goes back into its linear region.

ZERO CURRENT DETECTION AND TRIGGERING BLOCK (see fig. 5)
S6500 operates as a critical conduction current mode controller. The zero current detector switches on the external MOSFET as the voltage across the boost inductor reverses, just after the current through the boost inductor has gone to zero. The slope of the inductor current is indirectly detected by monitoring the voltage across an auxiliary winding and connecting it to the zero current detector Pin 5.
Once the inductor current reaches ground level, the polarity of the voltage across the winding is reversed.
When the Idet input falls below 1.5V, the comparator output is triggered to the low state.
To prevent false tripping, 0.5V hysteresis is provided. The zero current detector input is protected internally by two clamps. The upper 7.0V clamp prevents input over voltage breakdown while the lower 0.7V clamp prevents substrate injection.
An internal current limit resistor protects the lower clamp transistor in case the Idet pin is shorted to ground accidentally. A watchdog timer function is added to the IC to eliminate the need for an external oscillator when used in stand-alone applications.

Figure 5. Zero Current Detection, Triggering and Disable Block.



MULTIPLIER BLOCK (see fig. 6)

A single quadrant, two input multiplier is the critical element that enables this device to get power factor correction. One input of multiplier(Pin 3) is connected to an external resistor divider which monitors the rectified ac line voltage. The other input is internally driven by a DC voltage which is the difference between error amplifier output (Pin 2) and reference voltage, Vref. The multiplier is designed to have an extremely linear transfer curve over a wide dynamic range, 0V to 3.8V for Pin 3, and 2.25V to 6V for error amplifier output under all line and load conditions.

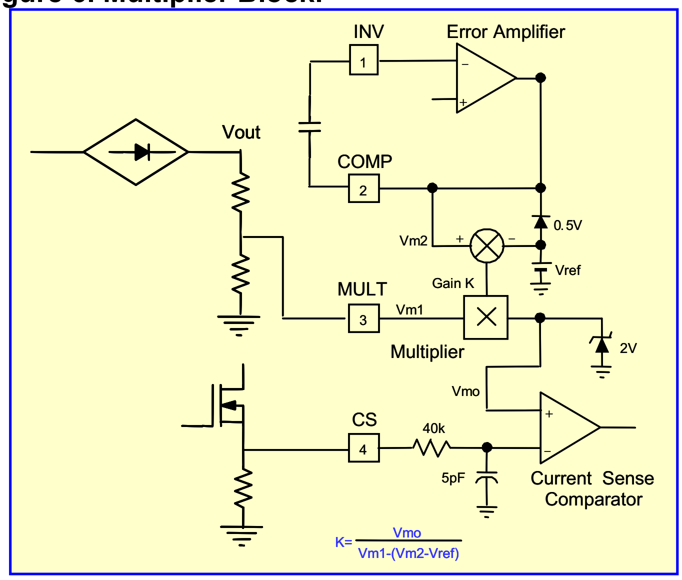
The multiplier output controls the current sense comparator threshold voltage as the ac voltage traverses sinusoidally from zero to peak line. This allows the inductor peak current to follow the ac line thus forcing the average input current to be sinusoidal. In other words, this has the effect of forcing the MOSFET on-time to track the input line voltage, resulting in a fixed drive output on-time, thus making the pre-converter load appear to be resistive to the ac line.

The equation below describes the relationship between multiplier output and its inputs.

$V_{mo} = K \times V_{m1} \times (V_{m2} - V_{ref})$

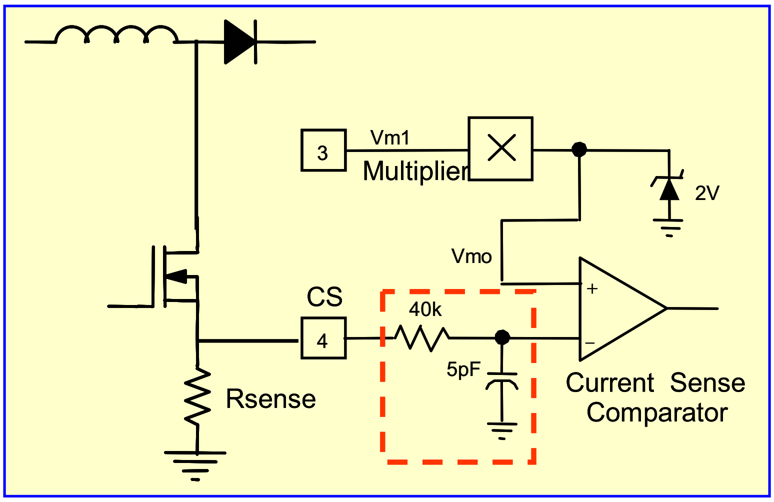
K : Multiplier gain, Vm1: Voltage at Pin 3, Vm2: Error amp output voltage, Vmo: Multiplier output voltage

Figure 6. Multiplier Block.



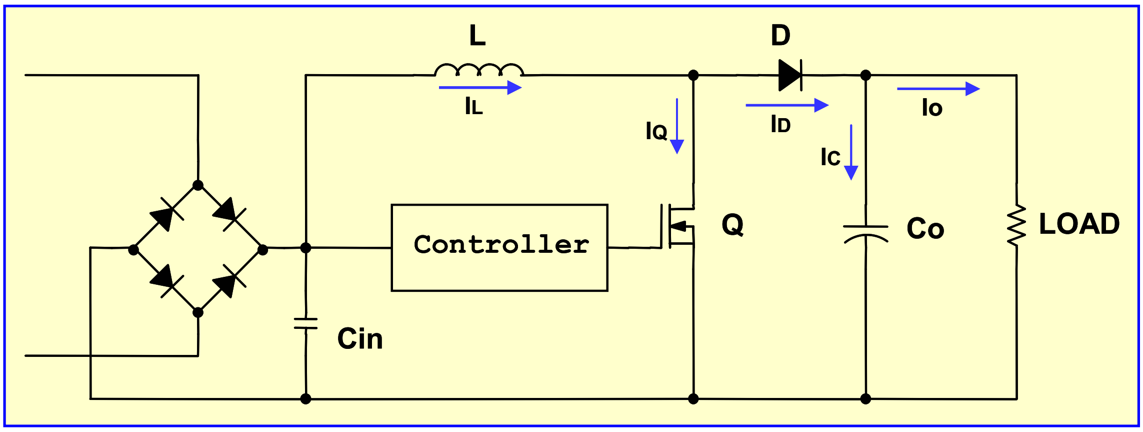
CURRENT COMPARATOR AND PWM LATCH (see fig.7):
The current sense comparator adopts the RS latch configuration to ensure that only a single pulse appears at the drive output during a given cycle. MOSFET drain current is sensed using an external sense resistor in series with the external MOSFET. When the sensed voltage exceeds the threshold set by the multiplier output, the current sense comparator turns off the MOSFET and resets the PWM latch.
The latch ensures that the output remains in a low state after the MOSFET drain current falls back to zero.
The peak inductor current under the normal operating condition is controlled by the multiplier output, Vmo.
The abnormal operating condition occurs during pre-converter start-up at extremely high line or as output voltage sensing is lost. Under these conditions, the multiplier output and current sense threshold will be internally clamped to 2.0V.
Therefore, the maximum peak switch current is limited to : Ipk(max) = 2.0V / Rsense
In the S6500, an internal R/C filter has been included to attenuate any high frequency noise that may be present on the current waveform. This circuit block eliminates the need for an external R/C filter otherwise required for proper operation of the circuit.

Figure 7. Current Sense Comparator.



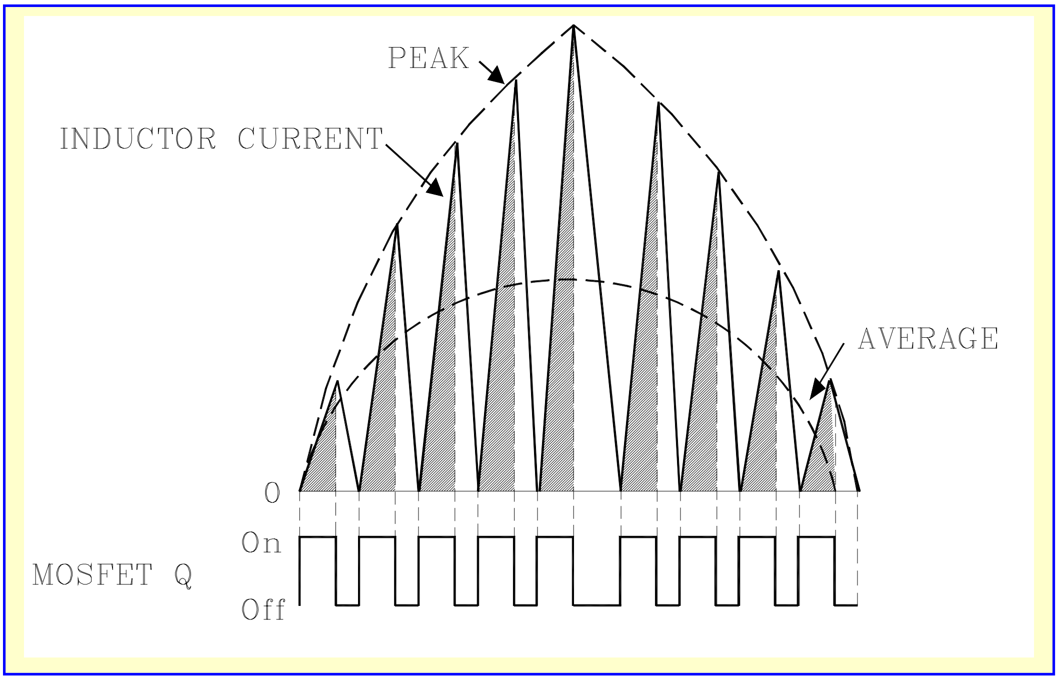
DRIVER
The S6500 contains a single totem-pole output stage designed specifically for a direct drive of power MOSFET. The drive output is capable of up to 500mA peak current with a typical rise and fall time of 100ns, 50ns respectively with a 1.0nF load.
Additional circuitry has been added to keep the drive output in a sinking mode whenever the UVLO is active. This characteristic eliminates the need for an external gate pull-down resistor.
Internal voltage clamping ensures that the output driver is always lower than 14V when supply voltage exceeds the rated Vgs of the external MOSFET.
This eliminates an external zener diode and extra power dissipation associated with it that otherwise is required for the reliable circuit operation.

TM PFC Operation (Boost Topology)
The operation of the PFC Transition Mode controlled boost converter, can be summarized in the following description. The AC mains voltage is rectified by a diode bridge and the rectified voltage delivered to the boost converter. This, using a switching technique, boosts the rectified input voltage to a regulated DC output voltage(Vo). The boost converter consists of a boost inductor (L), a controlled power switch (Q), a catch diode (D), an output capacitor (Co) and, obviously, a control circuitry (see fig. 8).
The goal is to shape the input current in a sinusoidal fashion, in-phase with the input sinusoidal voltage. To do this the S6500 uses the so-called Transition Mode technique.
Figure 8. Boost Converter Circuit.



The error amplifier compares a partition of the output voltage of the boost converter with an internal reference, generating a signal error proportional to the difference between them.
If the bandwidth of the error amplifier is narrow enough (say, below 20 Hz), the error signal is a DC value over a given half-cycle. The error signal is fed into the multiplier block and multiplied by a partition of the rectified mains voltage. The result will be a rectified sinusoid whose peak amplitude depends on the mains peak voltage and the value of the error signal.
The output of the multiplier is in turn fed into the (+) input of the current comparator, thus it represents a sinusoidal reference for PWM. In fact, as the voltage on the current sense pin (istantaneous inductor current times the sense resistor) equals the value on the (+) of the current comparator, the conduction of the external MOSFET is terminated. As a consequence, the peak inductor current will be enveloped by a rectified sinusoid. It is possible to prove also that this operation produces a costant ON-time over each line half-cycle (see "Boost Inductor"). After the MOSFET has been turned off, the boost inductor discharges its energy into the load until its current goes to zero. The boost inductor has now run out of energy, the drain node is floating and the inductor resonates with the total capacitance of the drain.
The drain voltage drops rapidly below the instantaneous line voltage and the signal on ZCD drives the MOSFET on again and another conversion cycle starts.
This low voltage across the external MOSFET at turn-on reduces both the switching losses and the equivalent drain capacitance energy that is dissipated inside the external MOSFET.
The resulting inductor current and the timing intervals of the MOSFET are shown in fig. 10, where it is also shown that, by geometric relationships, the average input current (the one which will be drawn from the mains) is just one-half of the peak inductor current waveform.
The system operates (not exactly on but very close to) the boundary between continuous and discontinuous current mode and that is why this system is called a Transition Mode PFC. Besides the simplicity and the few external parts required, this system minimizes the inductor size due to the low inductance value needed. On the other hand, the high current ripple on the inductor involves high RMS current and high noise on the rectified main bus, which needs a heavier EMI filter to be rejected.
These drawbacks limit the use of the TM PFC to lower power range applications.

Figure 9. Inductor Current waveform and MOSFET timing



Design Criteria

Here below some design criteria are described. The basic design specification concerns the following data:

- Mains Voltage Range: Virms(min) - Virms(max)
- Regulated DC Output Voltage: Vo
- Rated Output Power: Po
- Minimum Switching Frequency: $f$sw
- Maximum Output Voltage ripple: ΔVo
- Maximum Overvoltage admitted: ΔVOVP

For reference, it is useful to define also the following quantities:

- Expected efficiency: η
- Input Power: Pi (= Po/η)
- Maximum Mains RMS current: Irms (= Pi/Virms(min))
- Rated Output Current: Io (= Po/Vo)

POWER SECTION DESIGN

Input Bridge

The input diodes bridge can use standard slow recovery, low-cost devices. The quantities to consider will be just the input current (Irms), the maximum peak mains voltage and the thermal data of the diodes.

Input Capacitor

The input high frequency filter capacitor (Cin) has to attenuate the switching noise due to the high frequency inductor current ripple (twice the average line current, see fig. 8).

The worst conditions will occur on the peak of the minimum rated input voltage.

The maximum high frequency voltage ripple is usually imposed between 1% and 10% of the minimum rated input voltage. This is expressed by a coefficient r (typically, r = 0.01 to 0.1):

$$C_{IN} = \frac{I_{rms}}{2\pi \cdot f_{sw} \cdot r \cdot V_{irms(min)}}$$

High values of Cin alleviate the burden to the EMI filter but cause the power factor and the harmonic contents of the mains current to worsen, especially at high line and light load. On the other hand, low values of Cin improve power factor and reduce mains current distortion but require heavier EMI filtering and increase power dissipation in the input bridge. It is up to the designer to find the right trade-off in their application.

Output Capacitor

The output bulk capacitor (Co) selection depends on the DC output voltage, the admitted overvoltage, the output power and the desired voltage ripple. The 100 to 120Hz (twice the mains frequency) voltage ripple (ΔVO= 1/2 ripple peak-to-peak value) is a function of the capacitor impedance and the peak capacitor current ($I_{C(2f)pk} = I_o$):

$$\Delta V_o = I_o \sqrt{\frac{1}{(2\pi \cdot 2f \cdot C_o)^2} + ESR^2}$$

With a low ESR capacitor the capacitive reactance is dominant, therefore:

$$C_o \geq \frac{I_o}{4\pi \cdot f \cdot \Delta V_o} = \frac{P_o}{4\pi \cdot f \cdot \Delta V_o \cdot V_o}$$

ΔV_o is usually selected in the range of 1 to 5% of the output voltage.

Although ESR usually does not affect the output ripple, it has to be taken into account for power losses calculation. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

$$I_{Crms} = \sqrt{\frac{32\sqrt{2}}{9\pi} * I_{rms}^2 \frac{V_{irms}}{V_o} - I_o^2}$$

If the application has to guarantee a specified hold-up time, the selection criterion of the capacitance will Change : Co has to deliver the output power for a certain time (t_{Hold}) with a specified maximum dropout voltage:

$$Co = \frac{2 \cdot P_O \cdot t_{Hold}}{V_{o\_min}^2 - V_{op\_min}^2}$$

where Vo_min is the minimum output voltage value (which takes load regulation and output ripple into account) and Vop_min is the minimum output operating voltage before the 'power fail' detection from the downstream system supplied by the PFC.

BOOST INDUCTOR DESIGN

Designing the boost inductor involves several parameters and different approaches can be used.
First, the inductance value must be defined. The inductance (L) is usually determined so that the minimum switching frequency is greater than the maximum frequency of the internal starter, to ensure a correct TM operation. Assuming unity PF, it is possible to write:

$T_S = T_{on} + T_{off}$

$$T_{on} = \frac{L \cdot I_{Lpk} \cdot \sin(\theta)}{\sqrt{2} \cdot V_{i_{rms}} \cdot \sin(\theta)} = \frac{L \cdot I_{Lpk}}{\sqrt{2} \cdot V_{irms}} \qquad T_{off} = \frac{L \cdot I_{Lpk} \cdot \sin(\theta)}{Vo - \sqrt{2} \cdot V_{irms} \cdot \sin(\theta)}$$

being Ton and Toff the ON-time and the OFF-time of the power MOSFET respectively, ILpk the maximum peak inductor current in a line cycle and θ the instantaneous line phase ($\theta \in (0, \pi)$).
Note that the ON-time is constant over a line cycle. As previously said, ILpk is twice the line-frequency peak current, which is related to the input power and the line voltage:

$$ILpk = 2 \cdot \sqrt{2} \cdot \frac{Pi}{Virms}$$

Substituting this relationship in the expressions of Ton and Toff, after some algebra it is possible to find the instantaneous switching frequency along a line cycle:

$$fsw(\theta) = \frac{1}{Ton + Toff} = \frac{1}{2 \cdot L \cdot Pi} * \frac{Virms^2 \cdot (VO - \sqrt{2} \cdot Virms \cdot \sin(\theta))}{Vo}$$

The switching frequency will be minimum at the top of the sinusoid ($\theta = \pi/2 \Rightarrow \sin(\theta) = 1$), maximum at the zero crossings of the line voltage ($\theta = 0$ or $\pi \Rightarrow \sin(\theta) = 0$) where Toff = 0.
The absolute minimum frequency $f_{sw(min)}$ can occur at either the maximum or the minimum mains voltage, thus the inductor value is defined by:

$$L = \frac{V_{irms}^2 \cdot (V_O - \sqrt{2} \cdot V_{irms})}{2 \cdot f_{sw\,(min)} \cdot P_i \cdot V_O}$$

where Virms can be either Virms(min) or Virms(max), whichever gives the lower value for L.

AUXILIARY WINDING DESIGN

The auxiliary winding voltage is lowest at the highest line. So the number of auxiliary winding can be obtained by.

$$N_{aux} = \frac{V_{cc} \cdot N_P}{V_O - \frac{2\sqrt{2}}{\pi} V_{in(HL)}}$$

POWER MOSFET DESIGN

The choice of the MOSFET concerns mainly its R_{DSon}, which depends on the output power, since the breakdown voltage is fixed just by the output voltage, plus the overvoltage admitted and a safety margin. The MOSFET's power dissipation depends on conduction and switching losses.
The conduction losses are given by:

$$P_{ON} = I_{Qrms}{}^{2} \cdot R_{DSon}$$

where:

$$I_{Qrms} = 2 \cdot \sqrt{2} \cdot I_{rms} \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} * \frac{V_{irms}}{V_O}}$$

The switching losses due to current-voltage cross occur only at turn-off because of the TM operation:

$$P_{CROSS} = V_O \cdot I_{rms} \cdot t_{fall} \cdot f_{sw},$$

where t_{fall} is the crossover time at turn-off. At turn-on the loss is due to the discharge of the total drain capacitance inside the MOSFET itself. In general, these losses are given by:

$$P_{CAP} = (3.3 \cdot C_{oss} \cdot V_{DRAIN}{}^{1.5} + (1/2) \cdot C_d \cdot V_{DRAIN}{}^{2}) \cdot f sw$$

where C_{oss} is the internal drain capacitance of the MOSFET (@ V_{DS} = 25V), C_d is the total external drain parasitic capacitance and V_{DRAIN} is the drain voltage at MOSFET turn-on.
In practice it is possible to give only a rough estimate of the total switching losses because both $f$sw and VDRAIN change along a given line half-cycle. VDRAIN, in particular, is affected not only by the sinusoidal change of the input voltage but also by the drop due to the resonance of the boost inductor with the total drain capacitance (see fig. 11). This causes, at low mains voltage, V_{DRAIN} to be zero during a significant portion of each line half-cycle.
It is possible to show that "Zero-Voltage-Switching" occurs as long as the instantaneous line voltage is less than half the output voltage.
the MOSFET gate drive resistor is determined by

$$R_g > (V_{omax} / I_{omax}) = (16V / 500mA) = 32\Omega$$

The value is calculated on the assumption that the gate-source voltage should be a square waveform, i.e, abrupt changes with no rising or falling time. Thus the drive current can not reach 500mA during the rising or falling time although R_g of 32Ω is used. 10Ω is recommended as the Rg in order to the MOSFET switching loss. The experimental results show that the gate peak current goes up to 300mA with 10Ω.

BOOST DIODE DESIGN

The boost freewheeling diode will be a fast recovery one. The value of its DC and RMS current, useful for losses computation, are respectively:

$$I_{Do} = I_o$$

$$I_{Drms} = 2 \cdot \sqrt{2} \cdot I_{rms} \sqrt{\frac{4\sqrt{2}}{9\pi} * \frac{V_{irms}}{V_O}}$$

The conduction losses can be estimated as follows:

$$P_{DON} = V_{to} \cdot I_{Do} + R_d \cdot I_{Drms}^2$$

where V_{to} (threshold voltage) and Rd (differential resistance) are parameters of the diode.
The breakdown voltage is fixed with the same criterion as the MOSFET.

S6500 Biasing Circuitry (pin by pin)

Please, refer to the schematic circuit shown in fig. 12.

Pin 1 (INV) ;

leads both to the inverting input of the E/A and to the OVP circuit. A resistive divider will be connected between the regulated output voltage of the boost and the pin. The internal reference on the non-inverting input of the E/A is 2.5V and the OVP alarm level current is 40μA.
R11+ R12 and R13 will be then selected as follow:

$$\frac{R11 + R12}{R13} = \frac{V_O}{2.5V} - 1 \qquad R11 + R12 = \frac{\triangle V_{OVP}}{40uA}$$

Pin 2 (COMP) ;

the feedback loop bandwidth must be narrower than 30Hz for the PFC application. Therefore a capacitor is connected between INV and EA_OUT to eliminate the 120Hz ripple voltage by 40dB.
to improve the power factor, Ccomp must be increased than the calculated value. And to improve the system response, Ccomp must be lowered than the calculated value.

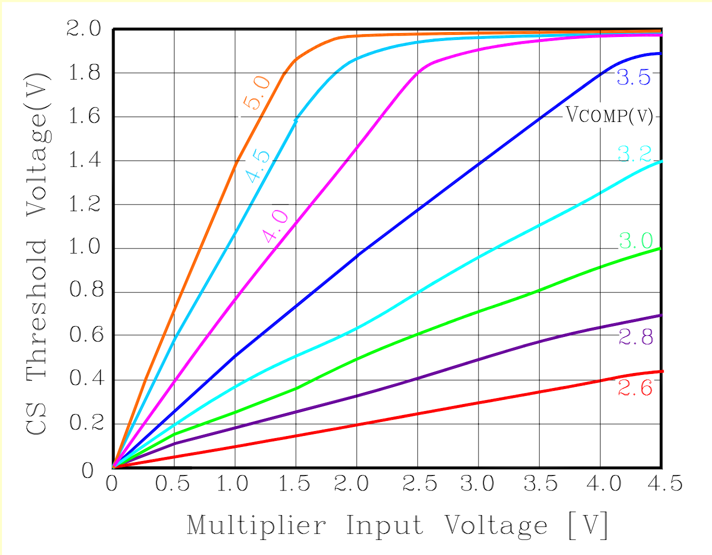
$$BW = \frac{1}{2\pi \quad RC} = \frac{1}{2\pi \quad RC} = 30Hz$$

Pin 3 (MULT) ;
the second multiplier input. It will be connected, through a resistive divider, to the rectified mains to get a sinusoidal voltage reference. The multiplier can be described by the relationship:

$$V_{CS} = k \cdot (V_{COMP} - 2.5V) \cdot V_{MULT}$$

where VCS (Multiplier output) is the reference for the current sense, k is the multiplier gain, V_{COMP} is the voltage on pin 2 (E/A output) and VMULT is the voltage on pin 3.
A complete description is given by the diagram of fig. 10, which shows the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed inside the range 0 to 3V of V_{MULT} and the range 0 to 1.6V of VCS, while the minimum guaranteed value of the maximum slope of the characteristics family ($\Delta V_{CS}/\Delta V_{MULT}$) is 1.65. Taking this into account, the following is the suggested procedure to set properly the operating point of the multiplier.

Figure 10. Multiplier characteristics family



First, the maximum peak value for V_{MULT}, $V_{MULTpkx}$, is selected. This value, which will occur at maximum mains voltage, should be 3V or nearly so in wide range mains and less in case of single mains.
The minimum peak value, occurring at minimum mains voltage will be:

$$V_{MULTpkmin} = V_{MULTpkx} \frac{V_{irms(min)}}{V_{irms(max)}}$$

This value, multiplied by the minimum guaranteed (ΔV_{CS} / ΔV_{MULT}) will give the maximum peak output voltage of the multiplier:

$$V_{XCSpk} = 1.65 \cdot V_{MULTpkmin}$$

If the resulting V_{XCSpk} exceeds the linearity limit of the current sense (1.6V), the calculation should be repeated beginning with a lower $V_{MULTpkx}$ value. In this way, the divider will be such that:

$$\frac{R3}{R1 + R2 + R3} = \frac{V_{MULTpkx}}{\sqrt{2} \cdot V_{irms(max)}}$$

the individual values can be chosen by setting the current through R3, in the hundreds µA or less to minimize power dissipation.

Pin 4 (CS) ;

the inverting input of the current sense comparator. Through this pin, the S6500 reads the instantaneous inductor current, converted to a proportional voltage by an external sense resistor (Rs).
As this signal crosses the threshold set by the multiplier output, the PWM latch is reset and the power MOSFET is turned off. The MOSFET will stay in OFF-state until the PWM latch is set again by the ZCD signal. An internal circuit ensures that the PWM latch cannot be set until the signal on pin 4 has disappeared.
The sense resistor value is calculated as follows:

$$R_S \leq \frac{V_{XCSpk}}{I_{Rspk}}$$

where V_{XCSpk} has been calculated as per described earlier and:

$$I_{Rspk} = 2\sqrt{2} \cdot I_{rms}$$

The power dissipated in Rs, is given by:

$$P_{Rs} = Rs \cdot I_{Qrms}^{\ 2} .$$

The internal 2.0V (max.) zener clamp on the non-inverting input of the PWM comparator sets a current limitation threshold, so that the maximum current through Rs can be as high as:

$$I_{Rspkmax} = 2.0 / R_S$$

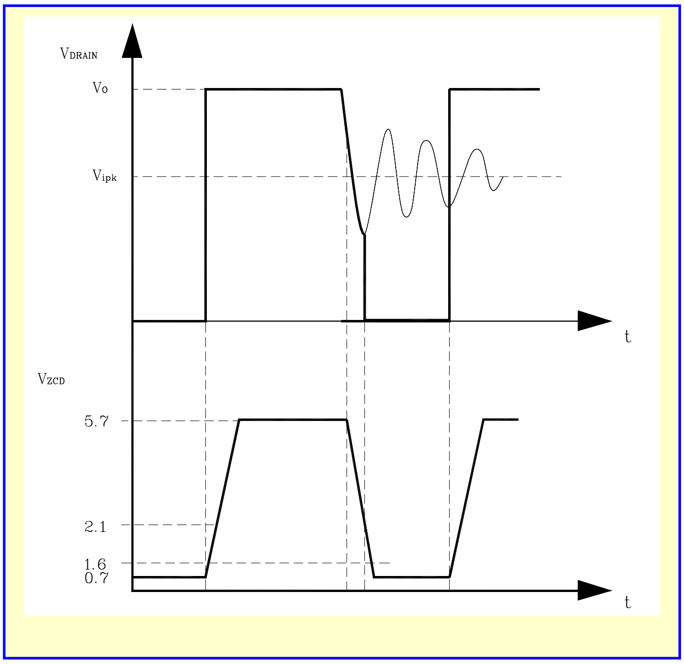
This will be the maximum inductor current as well, therefore one must make sure that the boost inductor does not saturate at this current level, which is very likely to be reached when the boost converter is powered on (especially at low line) or powered off.

Pin 5 (ZCD) ;
the input to the Zero Current Detector circuit. The ZCD pin will be connected to the auxiliary winding of the boost inductor through a limiting resistor. The ZCD circuit is negative-going edge-triggered: when the voltage on the pin falls below 1.5 V the PWM latch is set and the MOSFET is turned on. To do so, however, the circuit must be armed first: prior to falling below 1.5V the voltage on pin 5 must experience a positive - going edge exceeding 2.0 V (due to MOSFET's turn-off).
The maximum main-to-auxiliary winding turn ratio, m, has to ensure that the voltage delivered to the pin during MOSFET's OFF-time is sufficient to arm the ZCD circuit. Then:

$$m \leq \frac{V_O - \sqrt{2} \cdot V_{irms\,(max.)}}{2.0}$$

If the winding is used also for supplying the IC, the above criterion may not be compatible with the Vcc voltage range. To solve this incompatibility the self-supply network shown in the schematic of fig. 12 can be used. The minimum value of the limiting resistor can be found assuming 3 mA current through the pin and considering the maximum voltage (the absolute value) across the auxiliary winding. The actual value can be then fine-tuned trying to make the turn-on of the MOSFET occur exactly on the valley of the drain voltage oscillation (the boost inductor, completely discharged, is ringing with the drain capacitance, see fig. 11). This will minimize the power dissipation at turn-on.

Figure 11. Optimum MOSFET Turn-on



If the pin is driven by an external signal, the S6500 will be synchronized to (the negative-going edges of) that signal. If left floating, the S6500 will work at the frequency of its internal starter. Obviously, neither TM operation will take place nor high PF will be achieved in this case, but these characteristics can be exploited in applications other than PFC.

Pin 6 (GND) ;
This pin acts as the current return both for the signal internal circuitry and for the gate drive current. When layouting the printed circuit board, these two paths should run separately.

Pin 7 (OUT)
the gate driver output. The pin is able to drive an external MOSFET with 500mA source and sink capability. to avoid undesired switch-on of the external MOSFET because of some leakage current when the supply of the chip is below the UVLO threshold, an internal pull-down circuit holds the pin low.
The circuit guarantees 0.3V maximum on the pin (@ Isink = 10mA), with Vcc > 3V. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET used to this purpose.

Pin 8 (Vcc)
the supply of the device. This pin will be externally connected to the start-up circuit (usually, one resistor connected to the rectified mains) and to the self-supply circuit.
Whatever the configuration of the self-supply system, a capacitor will be connected between this pin and ground. to start the S6500, the voltage must exceed the start-up threshold (11.5V max.).
Below this value the device does not work and consumes less than 30μA from Vcc.
This allows the use of high value start-up resistors (in the hundreds kΩ), which reduces power consumption and optimises system efficiency at low load, especially in wide range mains applications.
When operating, the current consumption (of the device only, not considering the gate drive current) rises to a value depending on the operating conditions but never exceeding 4.0mA.
The device keeps on working as long as the supply voltage is over the UVLO threshold (9.5V max).
If the Vcc voltage exceeds 18V an internal zener diode, 35mA rated, will be activated that clamps the voltage. In that case the power consumption of the device will increase considerably, but there is no harm as long as the current is below the maximum rating.

DESIGN EXAMPLE
A 80W converter is designed to illustrate the design procedure. The system parameters are as follows.

- Maximum output power : 80W
- Input voltage range : 85Vrms~265Vrms
- Output voltage : 400V
- AC line frequency : 60Hz
- PFC efficiency : 90%
- Minimum switching frequency : 33kHz
- Input capacitor ripple voltage : 24V
- Output voltage ripple : 20V
- OVP set voltage : 460V

POWER MOSFET:
Two parameters are useful to select the suitable device: the minimum blocking voltage $V_{(BR)DSS}$ and the R_{DSON} because of power dissipation.
The device selected is the STK0675 ($V_{(BR)DSS}$ = 650V, I_D = 7A, R_{DSON} = 1.2Ω).

BOOST DIODE (D1):
The plastic axial diode BYV26 (1000V / 1A) has been selected.

BOOST INDUCTOR (T):
The boost inductor is determined by (BOOST INDUCTOR DESIGN). Calculate it at both the lowest line and the highest line and choose the lower value. The calculated value is 1.3mH. To get the calculate inductor value, EI3026 core is used and the primary winding is 75 turns. The air gap is 0.80mm at both legs of the EI core. The auxiliary winding is determined by (AUXILIARY WINDING DESIGN) and the auxiliary winding is 6 turns.

OUTPUT FILTER CAPACITOR (C9):
The specification on the output voltage ripple determines the capacitance value.
Assuming 50 Hz minimum line frequency, a 47μF/450V capacitor has been selected. This gives an output ripple $\Delta Vo = \pm 20V$.

MULTIPLIER SETTING (R1, R2, R3) AND SENSE RESISTOR (R9, R10):
The multiplier divider is selected so to exploit about 80% of its linear dynamics ($V_{MULTpkx}$ = 2.5V) as per the procedure described in pin 3 description. The sense resistor is then determined. As to R9 and R10, metal film resistors are suitable because of the high peak current flowing in it.

OUTPUT DIVIDER (R9, R10, R11):
R10 + R11 is selected so to achieve the desired overvoltage trip level (ΔVOVP = 60V), while R9 is chosen so to get the specified output regulated voltage.

ERROR AMPLIFIER COMPENSATION
The error amplifier has been compensated so as to get a type 2 amplifier that provides a pole at the origin and a zero-pole pair. As compared to a type1 amplifier (compensated with a single capacitor) this compensation offers a higher phase margin under all operating conditions and is therefore recommended when the PFC pre-regulator powers a DC-DC converter.
However, the twice-mains-frequency gain will be higher because of the zero, which causes a higher ripple at the output of the E/A and, as a result, a higher 3rd harmonic (and a higher THD) of the current drawn from the mains.

THD REDUCER
In the PCB there is provision for a network (see schematic of figure 12, in the dotted box) able to reduce the crossover distortion of the PFC input current, that is the small flat region appearing at the zero crossings of the mains voltage. The effect of this circuit is to force the ON-time of the power switch to increase nearby the zero-crossings. As a result, the energy inside the boost inductor will be greater and the deadtime during which there is no energy transfer is reduced. The circuit fine-tuning has to be made experimentally.

NTC
The NTC has been moved from the input to the output, in series with the boost diode. In this way, though still doing its job of inrush current limiter, it will undergo the output current instead of the input current, as in the typical position, with a considerable power dissipation reduction. The extra voltage on mosfet's drain while the boost diode is conducting is negligible.
The schematic circuit of fig. 12 shows the values of all the parts used. In fig. 13 the printed circuit board and the component layout of the demonstration board are shown.

Figure 12. 80W, Wide Range Demonstration Board(S6500) : Application circuit diagram

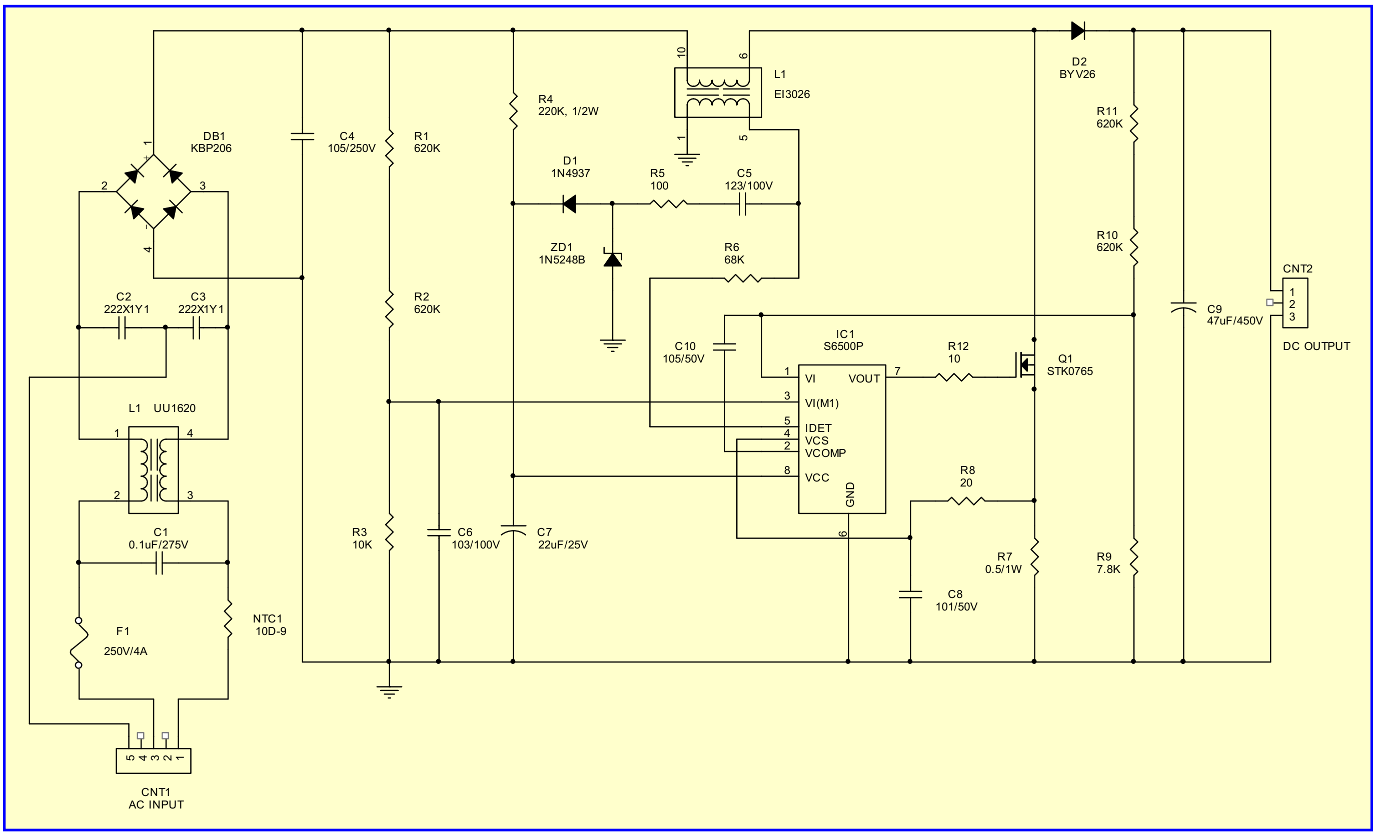
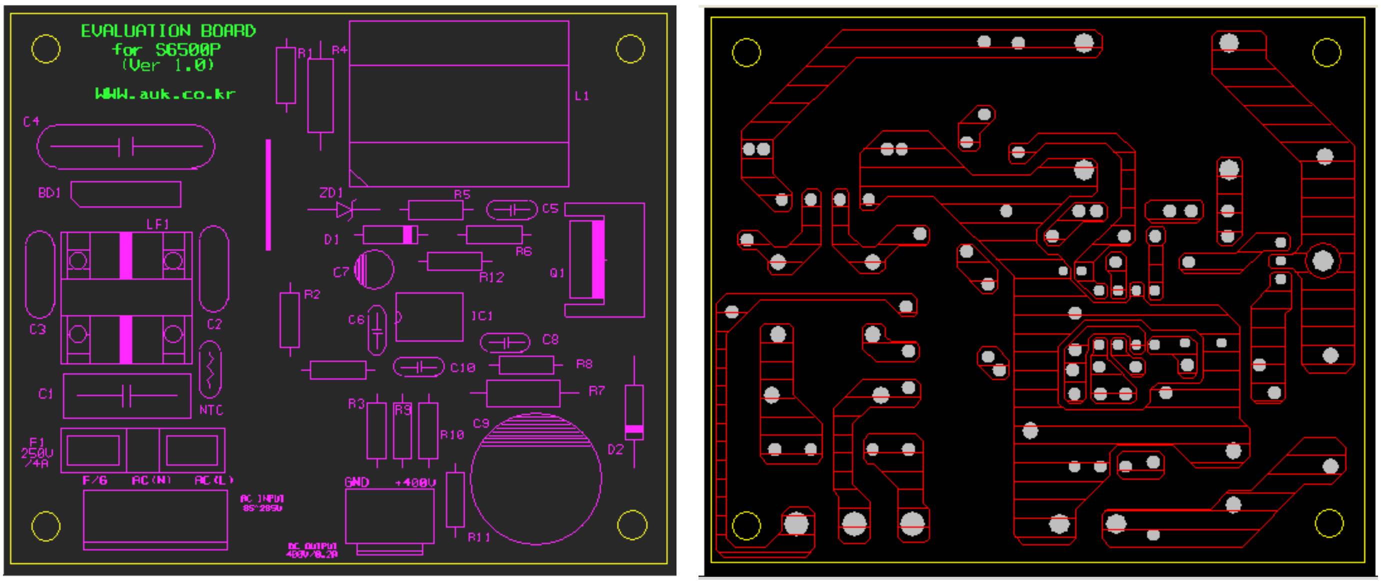


Figure 13. 80W : PCB and Component Layout (Top view, real size 75x90mm)



Boost Main Inductor Spec.

1. Winding Specification

No.	Pin(S-F)	Wire	Turns	Insulation	Remarks
Np	10 - 6	0.2ϕ * 10	75	PS Tape, t=0.05mm, 3T	Solenoid Winding
Ns	5 - 1	0.15ϕ	6	PS Tape, t=0.05mm, 1T	Space Winding

2. Electrical Characteristic

Closure	Pin	Spec.	Remarks
Inductance	10 - 6	1.3mH ±5%	1KHz, 1V
Leakage L			

3. Core & Bobbin
Core : EI3026, PL5(Samwha)
Bobbin : EI3026

S6500, 80W Wide Range Application Circuit Components List

Items	Part No.	Location No.	Specification	Items	Part No.	Location No.	Specification
PFC IC	S6500P	IC1	DIP-8	Capacitor	C-Myler	C4	630V / 104
MOSFET	STK0765	Q1	650V / 7.0A /1.2Ω	Capacitor	C-Myler	C5	100V / 123
Inductor	EI3026	L1	1.3mH / (75:6)	Capacitor	C-Myler	C6	100V / 103
Resistor	Carbon film	R1, R2	1/4W, 620kΩ J	Capacitor	C-Elc	C7	25V / 22uF
Resistor	Carbon film	R3	1/4W, 10kΩ J	Capacitor	C-Myler	C8	50V / 101
Resistor	Carbon film	R4	1W, 240kΩ J	Capacitor	C-Elc	C9	450V / 47µF φ 18×26
Resistor	Carbon film	R5	1/4W, 100Ω J	Capacitor	C-Myler	C10	50V / 105
Resistor	Carbon film	R6	1/4W, 68kΩ J	Bridge Diode	KBP206	BD1	600V / 2A
Resistor	Metal film	R7	1W, 0.5Ω F	FRD	1N4937	D1	600V / 1A
Resistor	Carbon film	R8	1/4W, 1kΩ J	FRD	BYV26EGP	D2	1000V / 1A
Resistor	Metal film	R9	1/4W, 7.8kΩ F	Zenner	1N5248B	ZD1	0.5W / 18V
Resistor	Metal film	R10, R11	1/4W, 620kΩ F	Line Filter	UU1160	LF1	-
Resistor	Carbon film	R12	1/4W, 10 Ω J	NTC		NTC1	-
Capacitor	PC × 2 335M	C1	275V 0.1µF	Fuse	4A 250V	F1	250V / 4A
Capacitor	C-Ceramic	C2, C3	250VAC 222X1Y1	Connector	YW396 - 05, 03	CNT1, CNT2	-